CPU Profile

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Contents

1. Scope

The DCIM CPU Profile describes the properties and interfaces for executing system management tasks related to the management of processors within a system. The profile standardizes and aggregates the description for the CPU properties into a CPU view representation as well as provides static methodology for the clients to query the CPU views without substantial traversal of the model.

2. Normative References

The following referenced documents are indispensable for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

- DMTF DSP1033, Profile Registration Profile 1.0.0 Dell Lifecycle Controller Best Practices Guide 1.0, http://en.community.dell.com/techcenter/extras/m/white_papers/20066173.aspx
- Dell WSMAN Licenses and Privileges 1.0
- DMTF DSP0226, Web Services for Management (WSManagement) Specification 1.1.0
- DMTF DSP0227, WSManagement CIM Binding Specification 1.0.0
- Dell Tech Center MOF Library http://www.delltechcenter.com/page/DCIM.Library.MOF
    - DCIM_CPUView.mof
    - DCIM_LCEnumeration.mof
    - DCIM_LCRegisteredProfile.mof

3. Terms and Definitions

For the purposes of this document, the following terms and definitions apply.

3.1. Conditional

Indicates requirements to be followed strictly in order to conform to the document when the specified conditions are met

3.2. Mandatory

Indicates requirements to be followed strictly in order to conform to the document and from which no deviation is permitted

3.3. May

Indicates a course of action permissible within the limits of the document

3.4. Optional

Indicates a course of action permissible within the limits of the document

3.5. Referencing profile

Indicates a profile that owns the definition of this class and can include a reference to this profile in its "Related Profiles" table

3.6. Shall

Indicates requirements to be followed strictly in order to conform to the document and from which no deviation is permitted.

3.7. FQDD

Fully Qualified Device Descriptor is used to identify a particular component in a system.

3.8. Interop Namespace

Interop Namespace is where instrumentation instantiates classes to advertise its capabilities for client discovery.

3.9. Implementation Namespace

Implementation Namespace is where instrumentation instantiates classes relevant to executing core management tasks.

3.10. ENUMERATE

Refers to WSMAN ENUMERATE operation as described in Section 8.2 of DSP0226_V1.1 and Section 9.1 of DSP0227_V1.0

3.11. GET

Refers to WSMAN GET operation as defined in Section 7.3 of DSP00226_V1.1 and Section 7.1 of DSP0227_V1.0

4. Symbols and Abbreviated Terms

4.1. CIM

Common Information Model

4.2. iDRAC

Integrated Dell Remote Access Controller – management controller for blades and monolithic servers

4.3. CMC

Chassis Manager Controller – management controller for the modular chassis

4.4. WBEM

Web-Based Enterprise Management

5. Synopsis

Profile Name: CPU

Version: 4.0.0

Organization: Dell

CIM Schema Version: 2.41 Final

Dell Schema Version: 1.0.0

Interop Namespace: root/interop

Implementation Namespace: root/dcim

Central Class: DCIM_CPUView

Scoping Class: DCIM_ComputerSystem

The Dell CPU Profile is a component profile that contains the Dell specific implementation requirements for CPU view.

DCIM_CPUView shall be the Central Class.

Table 1 identifies profiles that are related to this profile.

Table 1. Related Profiles

Profile Name	Organization	Version	Relationship
Profile Registration	DCIM	1.0	Reference

6. Description

The Dell CPU Profile describes platform's CPUs. Each CPU's information is represented by an instance of DCIM_CPUView class. Figure 1 details the class diagram of the Dell CPU Profile.

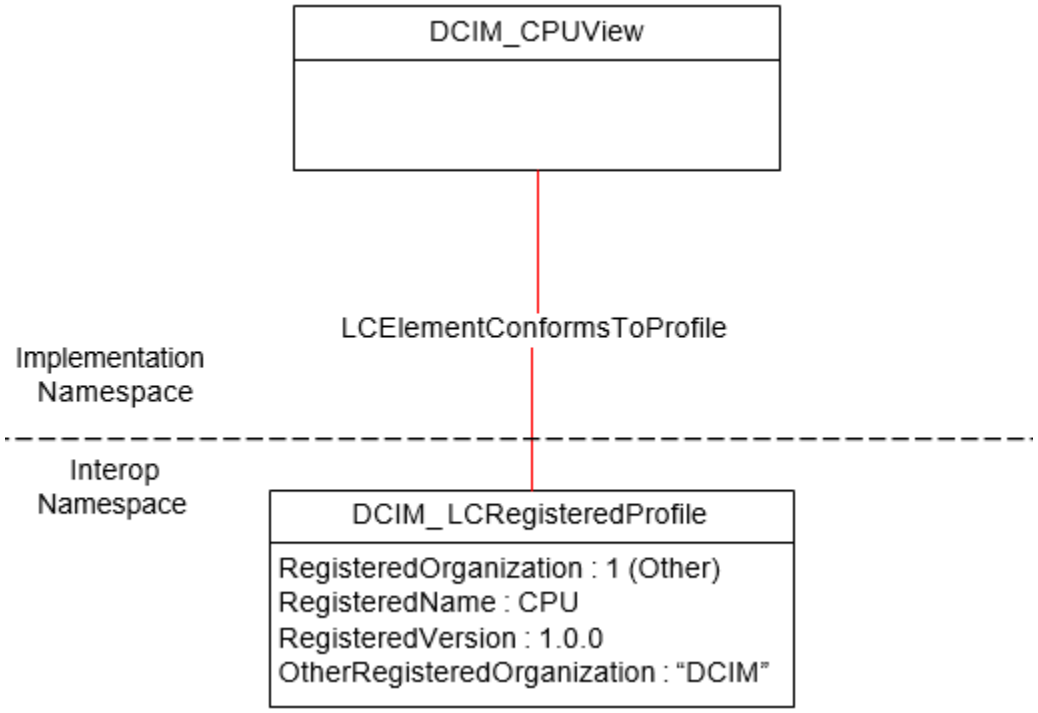

Figure 1. Class Diagram

Figure 2 details typical Dell CPU Profile implementation for a platform containing two CPUs. In order fo client to discover the instrumentation's support of this profile, CPUProfile is instantiated in the Interop Namespace. CPUProfile instance describes the information about the implemented profile: most importantly, the name and version of the profile and the organization name that produced the profile.

CPU1 and CPU2 are the CPU views representing the two CPUs in the Implementation Namespace. They are associated to the Interop namespace's CPUProfile instance.

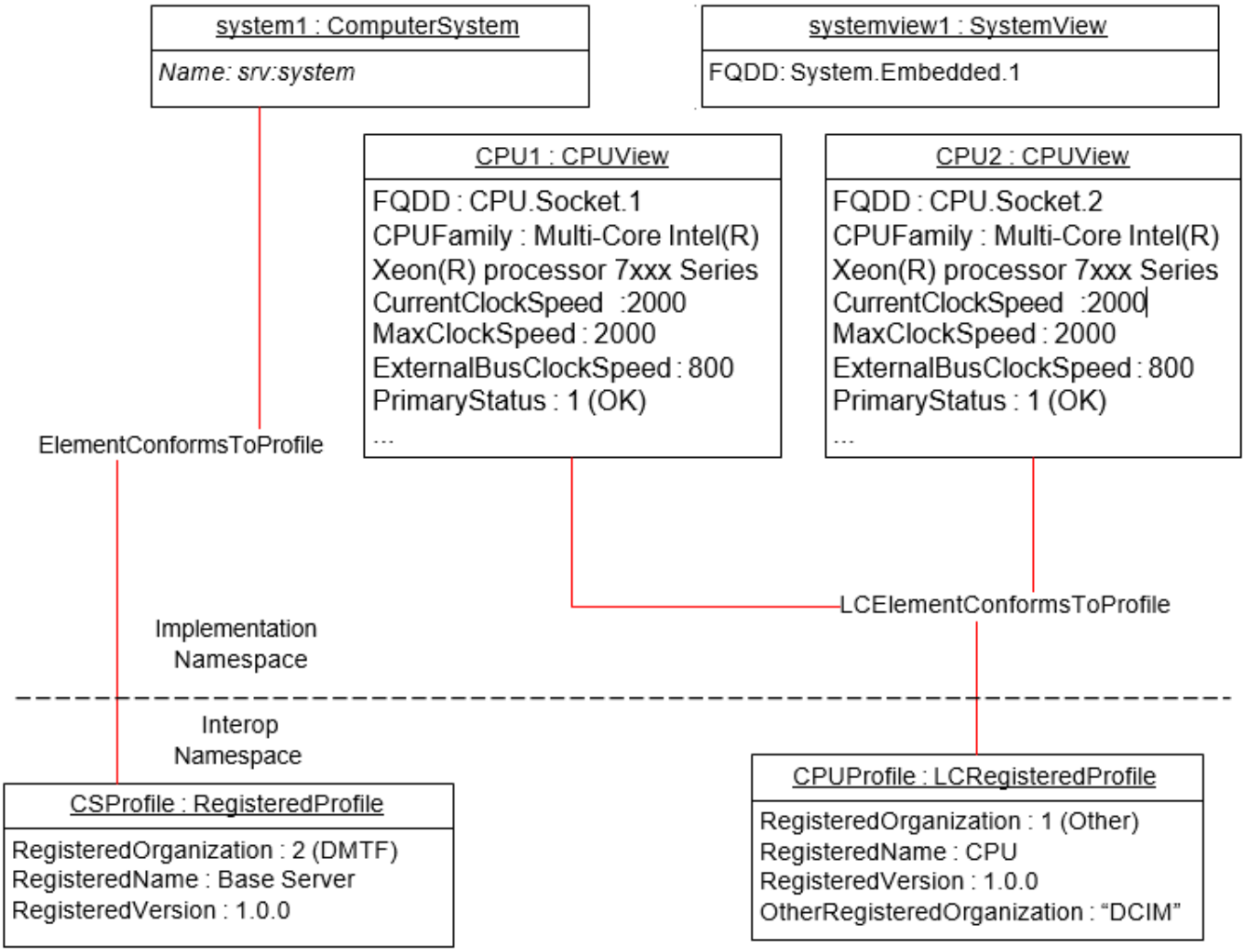

Figure 2. CPU Profile Implementation

7. Implementation Description

This section describes the requirements and guidelines for implementing Dell CPU Profile.

Table 2. Class Requirements: CPU Profile

Element Name	Requirement	Description
Classes		
DCIM_CPUView	Mandatory	The class shall be implemented in the Implementation Namespace. See section 7.1.
DCIM_LCElementConformsToProfile	Mandatory	The class shall be implemented in the Implementation Namespace.
DCIM_LCElementConformsToProfile	Mandatory	The class shall be implemented in the Interop Namespace.

Element Name	Requirement	Description
DCIM_LCRegisteredProfile	Mandatory	The class shall be implemented in the Interop Namespace. See section 7.2.
Indications		
None defined in this profile		

7.1. CPU View — DCIM_CPUView

This section describes the implementation for the DCIM_CPUView class. This class shall be instantiated in the Implementation Namespace.

The DCIM_LCElementConformsToProfile association(s) shall reference the DCIM_CPUView instance(s).

Note:– DCIM_CPUView gives the static inventory of CPUs. For real time status of CPUs, refer to DCIM_Sensor class.

7.1.1. Resource URIs for WinRM®

The class Resource URI shall be “http://schemas.dell.com/wbem/wscim/1/cim-schema/2/DCIM_CPUView?__cimnamespace=root/dcim”

The key property shall be the InstanceID.

The instance Resource URI for DCIM_CPUView instance shall be: “http://schemas.dell.com/wbem/wscim/1/cim-schema/2/DCIM_CPUView?__cimnamespace=root/dcim+InstanceID=<FQDD>”

7.1.2. Operations

The following table details the implemented operations on DCIM_CPUView.

Table 3. DCIM_CPUView - Operations

Operation Name	Requirements	Required Input
Get	Mandatory	Instance URI
Enumerate	Mandatory	Class URI

7.1.3. Properties

The following table details the implemented properties for DCIM_CPUView instance representing a processor in a system. The “Requirements” column shall denote the implementation requirement for the corresponding property. If the column “Property Name” matches the property name, the property either shall have the value denoted in the corresponding column “Additional Requirement”, or shall be implemented according to the requirements in the corresponding column “Additional Requirement”.

Table 4. DCIM_CPUView - Properties

Property Name	Requirements	Type	Requirement and Description
Cache1Associativity	Mandatory	uint16	An integer enumeration defining the system cache associativity: • "1" - "Unknown", • "2" - "Other", • "3" - "Direct Mapped" • "4" - "2-way Set-Associative", "5" - "4-way Set-Associative", "6" - "Fully Associative", • "7" - "8-way Set-Associative", "8" - "16-way Set-Associative", "9" - "12-way Set-Associative", "10" - "24-way Set-Associative", "11" - "32-way Set-Associative", "12" - "48-way Set-Associative", "13" - "64-way Set-Associative" "14" - "20-way Set-Associative"
Cache1ErrorMethodology	Optional	uint16	Cache ErrorMethodology - Contains the enumerated value that describes the cache's error detection/correction mechanism • "1" – Other • "2" – Unknown • "3" – None • "4" – Parity • "5" - Single-bit ECC • "6" -- Multi-bit ECC
Cache1Level	Mandatory	uint16	The cache level for Cache1 labeled cache. • "0" – L1 • "1" – L2 • "2" – L3 • "3" –L4 • "4" – L5 • "5" –L6 • "6" – L7 • "7" –L8
Cache1PrimaryStatus	Mandatory	uint32	Cache1PrimaryStatus provides a high level status value, intended to align with Red- Yellow-Green type representation of status. • "0" – Unknown • "1" – OK • "2" – Degraded • "3" – Error • "0x8000" - DMTF Reserved • "0xFFFF" - Vendor Reserved
Cache1Size	Mandatory	uint64	The property shall represent the total memory size of the cache in KBytes.

Property Name	Requirements	Type	Requirement and Description
Cache1SRAMType	Mandatory	uint16	Cache SRAM Type. • “1” – Other • “2” – Unknown • “4” -- Non-Burst • “8” – Burst • “16” -- Pipeline Burst • “32” – Synchronous • “64” -- Asynchronous
Cache1Type	Mandatory	uint16	Defines whether this is for instruction caching (value=3), data caching (value=4) or both (value=5, \"Unified\"). Also, \"Other\" (1) and \"Unknown\" (2) can be defined.
Cache1WritePolicy	Mandatory	uint16	Defines whether this is write-back (value=1) or write-through (value=0) Cache, or whether this information \"Varies with Address\" (2) or \"Unknown\" (3) can be specified.
Cache1Location	Mandatory	uint8	Specifies the location of cache • Internal • External • Reserved • Unknown
Cache2Associativity	Mandatory	uint16	An integer enumeration defining the system cache associativity: • “1” - “Unknown”, • “2” - “Other”, • “3” - “Direct Mapped” • “4” - “2-way Set-Associative”, “5” - “4-way Set-Associative”, “6” - “Fully Associative”, • “7” - “8-way Set-Associative”, “8” - “16-way Set-Associative”, “9” - “12-way Set-Associative”, “10” - “24-way Set-Associative”, “11” - “32-way Set-Associative”, “12” - “48-way Set-Associative”, “13” - “64-way Set-Associative” “14” - “20-way Set-Associative”
Cache2ErrorMethodology	Optional	uint16	Cache ErrorMethodology - Contains the enumerated value that describes the cache’s error detection/correction mechanism • “1” – other • “2” – Unknown • “3” – None • “4” – Parity • “5” -- Single-bit ECC • “6” - Multi-bit ECC

Property Name	Requirements	Type	Requirement and Description
Cache2Level	Mandatory	uint16	The cache level for Cache2 labeled cache. • “0” – L1 • “1” – L2 • “2” – L3 • “3” –L4 • “4” – L5 • “5” –L6 • “6” – L7 • “7” –L8
Cache2PrimaryStatus	Mandatory	uint32	Cache2PrimaryStatus provides a high level status value, intended to align with Red- Yellow-Green type representation of status. • “0” – Unknown • “1” – OK • “2” – Degraded • “3” – Error • “0x8000” - DMTF Reserved • “0xFFFF” - Vendor Reserved
Cache2Size	Mandatory	uint64	The property shall represent the total memory size of the cache in KBytes.
Cache2SRAMType	Mandatory	uint16	Cache SRAM Type. • “1” – Other • “2” – Unknown • “4” -- Non-Burst • “8” – Burst • “16” -- Pipeline Burst • “32” – Synchronous
Cache2Type	Mandatory	uint16	Defines whether this is for instruction caching (value=3), data caching (value=4) or both (value=5, \"Unified\"). Also, \"Other\" (1) and \"Unknown\" (2) can be defined.
Cache2WritePolicy	Mandatory	uint16	Defines whether this is write-back (value=1) or write-through (value=0) Cache, or whether this information \"Varies with Address\" (2) or \"Unknown\" (3) can be specified.
Cache2Location	Mandatory	uint8	Specifies the location of cache • Internal • External • Reserved • Unknown

Property Name	Requirements	Type	Requirement and Description
Cache3Associativity	Mandatory	uint16	An integer enumeration defining the system cache associativity: • "1" - "Unknown", • "2" - "Other", • "3" - "Direct Mapped" • "4" - "2-way Set-Associative", "5" - "4-way Set-Associative", "6" - "Fully Associative", • "7" - "8-way Set-Associative", "8" - "16-way Set-Associative", "9" - "12-way Set-Associative", "10" - "24-way Set-Associative", "11" - "32-way Set-Associative", "12" - "48-way Set-Associative", "13" - "64-way Set-Associative" "14" - "20-way Set-Associative"
Cache3ErrorMethodology	Optional	uint16	Cache ErrorMethodology - Contains the enumerated value that describes the cache's error detection/correction mechanism. • "1" – other • "2" – Unknown • "3" – None • "4" – Parity • "5" -- Single-bit ECC • "6" - Multi-bit ECC
Cache3Level	Mandatory	uint16	The cache level for Cache3 labeled cache. • "0" – L1 • "1" – L2 • "2" – L3 • "3" –L4 • "4" – L5 • "5" –L6 • "6" – L7 • "7" –L8
Cache3PrimaryStatus	Mandatory	uint32	Cache3PrimaryStatus provides a high level status value, intended to align with Red- Yellow-Green type representation of status. • "0" – Unknown • "1" – OK • "2" – Degraded • "3" – Error • "0x8000" - DMTF Reserved • "0xFFFF" - Vendor Reserved
Cache3Size	Mandatory	uint64	The property shall represent the total memory size of the cache in KBytes.

Property Name	Requirements	Type	Requirement and Description
Cache3SRAMType	Mandatory	uint16	Cache SRAM Type. • “1” – Other • “2” – Unknown • “4” -- Non-Burst • “8” – Burst • “16” -- Pipeline Burst • “32” – Synchronous
Cache3Type	Mandatory	uint16	Defines whether this is for instruction caching (value=3), data caching (value=4) or both (value=5, \"Unified\"). Also, \"Other\" (1) and \"Unknown\" (2) can be defined.
Cache3WritePolicy	Mandatory	uint16	Defines whether this is write-back (value=1) or write-through (value=0) Cache, or whether this information \"Varies with Address\" (2) or \"Unknown\" (3) can be specified.
Cache3Location	Mandatory	uint8	Specifies the location of cache • 0-Internal • External • Reserved • Unknown
Characteristics	Mandatory	uint32	The characteristics include certain features of the processor such as 64 bit support for data width of the processor. • “2” – Unknown • “4” - 64-bit Capable
CPUFamily	Mandatory	string	The property shall represent processor family type in hexadecimals.
CPUStatus	Mandatory	uint16	Indicates the current status of the Processor. For example, the Processor might be disabled due to a POST error (value=3). • “0” – Unknown • “1” - CPU Enabled • “2” - CPU Disabled by User • “3” - CPU Disabled By BIOS (POST Error) • “4” - CPU Is Idle “7” - Other
CurrentClockSpeed	Mandatory	uint32	The property value shall be in MHz. The current speed (in MHz) of this Processor.
ExternalBusClockSpeed	Mandatory	uint32	The property value shall be in MHz. The speed (in MHz) of the external bus interface (known as the front side bus).
FQDD	Mandatory	string	A string containing the Fully Qualified Device Description, a user-friendly name for the object.
InstanceID	Mandatory	string	The property value shall be the FQDD property value.
DeviceDescription	Mandatory	string	A string containing the friendly Fully Qualified Device Description,a property that describes the device and its location

Property Name	Requirements	Type	Requirement and Description
Manufacturer	Mandatory	string	The name of the organization responsible for producing the processor.
MaxClockSpeed	Mandatory	uint32	The property value shall be in MHz. The maximum speed (in MHz) of this Processor.
Model	Mandatory	string	The make and or model of the product
NumberofEnabledCores	Mandatory	uint32	Number of processor cores enabled for processor.
NumberofEnabledThreads	Mandatory	uint32	Total number of hardware enabled threads for processor. NOTE: The disabling of the multithreading by the BIOS does not affect the number of hardware enabled threads reported by this property.
NumberOfProcessorCores	Mandatory	uint32	Number of processor cores available for processor.
HyperThreadingEnabled	Mandatory	uint8	• 0-No • 1-Yes
HyperThreadingCapable	Mandatory	uint8	• 0-No • 1-Yes
VirtualizationTechnologyEnabled	Mandatory	uint8	• 0-No • 1-Yes
VirtualizationTechnologyCapable	Mandatory	uint8	• 0-No • 1-Yes
ExecuteDisabledEnabled	Mandatory	uint8	• 0-No • 1-Yes • 2 -- Not Applicable
ExecuteDisabledCapable	Mandatory	uint8	• 0-No • 1-Yes
TurboModeEnabled	Mandatory	uint8	• 0-No • 1-Yes
TurboModeCapable	Mandatory	uint8	• 0-No • 1-Yes
PrimaryStatus	Mandatory	uint32	PrimaryStatus provides a high level status value, intended to align with Red-Yellow- Green type representation of status. • “0” – Unknown • “1” – OK • “2” – Degraded • “3” – Error • “0x8000” - DMTF Reserved • “0xFFFF” - Vendor Reserved
Voltage	Mandatory	string	The property shall represent the voltage(s) of the processor in Volts.

Property Name	Requirements	Type	Requirement and Description
LastSystemInventoryTime	Mandatory	string	This property provides the last time \"System \"Inventory Collection On Reboot(CSIOR)\" was performed. The value is represented as yyyymmddHHMMSS.
LastUpdateTime	Mandatory	string	This property provides the last time the data was updated. The value is represented as yyyymmddHHMMSS

7.2. CPU Profile Registration

This section describes the implementation for the DCIM_LCRegisteredProfile class. This class shall be instantiated in the Interop Namespace.

The DCIM_LCElementConformsToProfile association(s) shall reference the DCIM_LCRegisteredProfile instance.

7.2.1. Resource URIs for WinRM®

The class Resource URI shall be "http://schemas.dmtf.org/wbem/wscim/1/cim-schema/2/CIM_RegisteredProfile?__cimnamespace=root/interop"

The key property shall be the InstanceID property.

The instance Resource URI shall be: “http://schemas.dell.com/wbem/wscim/1/cim-schema/2/DCIM_LCRegisteredProfile? cimnamespace=root/interop+InstanceID=DCIM:CPU:1.0.0”

7.2.2. Operations

The following table details the implemented operations on DCIM_LCRegisteredProfile.

Table 5. DCIM_LCRegisteredProfile - Operations

Operation Name	Requirements	Required Input
Get	Mandatory	Instance URI
Enumerate	Mandatory	Class URI

7.2.3. Properties

The following table details the implemented properties for DCIM_LCRegisteredProfile instance representing CPU Profile implementation. The “Requirements” column shall denote the implementation requirement for the corresponding property. If the column “Name” matches the property name, the property either shall have the value denoted in the corresponding column “Additional Requirements”, or shall be implemented according to the requirements in the corresponding column “Additional Requirements”.

Table 6. DCIM_LCRegisteredProfile

Property Name	Requirement	Type	Additional Requirements
InstanceID	Mandatory	String	DCIM:CPU:4.0.0
RegisteredName	Mandatory	String	This property shall have a value of "CPU".
RegisteredVersion	Mandatory	String	This property shall have a value of "4.0.0".
RegisteredOrganization	Mandatory	Uint16	This property shall have a value of 1 (Other).
OtherRegisteredOrganization	Mandatory	String	The property value shall match “DCIM”.

Property Name	Requirement	Type	Additional Requirements
AdvertisedTypes[]	Mandatory	Uint16	This property array shall contain [1(Other), 1 (Other)].
AdvertiseTypeDescriptions[]	Mandatory	String	This property array shall contain ["WS- Identify", "Interop Namespace"].
ProfileRequireLicense[]	Mandatory	String	This property array shall describe the required licenses for this profile. If no license is required for the profile, the property shall have value NULL.
ProfileRequireLicenseStatus[]	Mandatory	String	This property array shall contain the status for the corresponding license in the same element index of the ProfileRequireLicense array property. Each array element shall contain: • "LICENSED" • "NOT_LICENSED" If no license is required for the profile, the property shall have value NULL.

8. Methods

This section details the requirements for supporting extrinsic methods for the CIM elements defined by this profile.

No additional details specified.

9. Use Cases

See Lifecycle Controller (LC) Integration Best Practices Guide.

10. CIM Elements

No additional details specified.

11. Privilege and License Requirement

The following table describes the privilege and license requirements for the listed operations. For the detailed explanation of the privileges and licenses, refer to the Dell WSMAN Licenses and Privileges specification.

Table 7. Privilege and License Requirements

Class and Method	Operation	User Privilege Required	License Required
DCIM_CPUView	ENUMERATE, GET	Login	LM_REMOTE_ASSET_IN VENTORY
DCIM_LCElementConformsToProfile	ENUMERATE, GET	Login	None.
DCIM_LCRegisteredProfile	ENUMERATE, GET	Login	None.